What is claimed is:

1. A video signal processing apparatus comprising:

a plurality of line memories to which in sequence input video signal data is written on a line-by-line basis;

a timing controller for controlling a timing to write video signal data to the plurality of line memories and a timing to read video signal data from the plurality of line memories;

a computation output portion for computing video signal data read from the plurality of line memories and outputting video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction; and

a line controller which varies the pixel count in specified lines of video signal data obtained from the computation output portion, depending on a conversion rate of the video signal data resolution.

2. A video signal processing apparatus according to claim 1, the line controller further comprising:

a reference pixel count decision unit which decides a reference pixel count in the horizontal direction of video signal data obtained from the computation output portion, based on an elapsed period of time for a

specified number of lines of input video signal data and on a line count corresponding to the specified number of lines of video signal data obtained from the computation output portion; and

a pixel count variation unit which varies from the reference pixel count the pixel count in the specified lines of video signal data obtained from the computation output portion, depending on the conversion rate of the video signal data resolution.

3. A video signal processing apparatus according to claim 1, the line controller further comprising:

a reference pixel count decision unit which decides the reference pixel count in the horizontal direction of video signal data obtained from the computation output portion, by letting a difference be smaller than a specified period of time, the difference being a difference between an elapsed period of time for a specified number of lines of input video signal data and an elapsed period of time for the line count corresponding to the specified number of lines of video signal data obtained from the computation output portion;

a counting unit which counts the specified period of time; and

a pixel count variation unit which varies from the reference pixel count the pixel count in the horizontal direction of video signal data obtained from the

computation output portion if the count of the counting unit is equal to or smaller than the difference.

4. A video signal processing apparatus according to claim 2, wherein the reference pixel count decision unit decides the reference pixel count during vertical blanking interval of input video signal data, and wherein the pixel count variation unit then uses the reference pixel count for video signal data to be obtained from the computation output portion.

5. A video signal processing apparatus according to claim 1, wherein the plurality of line memories include at least three line memories, and wherein, while video signal data is written to one of the line memories, video signal data is read from the other line memories.

6. An integrated circuit comprising the video signal processing apparatus according to claim 1.

7. A method of processing video signal comprising:

writing in sequence input video signal data to a plurality of line memories on a line-by-line basis;

controlling a timing to write video signal data to the plurality of line memories and a timing to read video signal data from the plurality of line memories;

computing video signal data read from the plurality

of line memories and outputting video signal data differing in resolution which is determined by a pixel count in the horizontal direction and a line count in the vertical direction; and

varying the pixel count in specified lines of video signal data depending on a conversion rate of the video signal data resolution.

8. A method for processing video signal according to claim 7, further comprising:

deciding a reference pixel count in the horizontal direction of video signal data based on an elapsed period of time for a specified number of lines of input video signal data and on a line count corresponding to the specified number of lines of video signal data; and

varying from the reference pixel count the pixel count in the specified lines of video signal data depending on the conversion rate of the video signal data resolution.

9. A method of processing video signal according to claim 7, further comprising:

deciding the reference pixel count in the horizontal direction of video signal data, by letting a difference be smaller than a specified period of time, the difference being a difference in elapsed period of time for a specified number of lines of input video signal

data and elapsed period of time for the line count corresponding to the specified number of lines of the computed video signal data;

counting the specified period of time; and

varying from the reference pixel count the pixel count in the horizontal direction of the computed video signal data if the count is equal to or smaller than the difference.

10. A method for processing video signal according to claim 8, further comprising:

deciding the reference pixel count during vertical blanking interval of input video signal data, and

using the reference pixel count for the computed video signal data.

11. A method for processing video signal according to claim 7, wherein the plurality of line memories include at least three line memories, and wherein, while video signal data is written to one of the line memories, video signal data is read from the other line memories.